Abstract

Drive for a half-bridge inverter

The selection of the dead time in the case of a half-bridge inverter influences the efficiency thereof. The optimal dead time, and thus the optimal switching-on time of a lower half-bridge transistor (T2) is accomplished according to the invention by virtue of the fact that switching on is delayed until the current in a level shift transistor (T3) has dropped below a given threshold. A further aspect of the invention consists in that the delay in switching on the lower half-bridge transistor (T2) is immediately suppressed whenever a charging current flows in a trapezoidal capacitor, and this is accompanied by the rise of the half-bridge output voltage (UHB) after the traversal of a minimum.

Figure 4